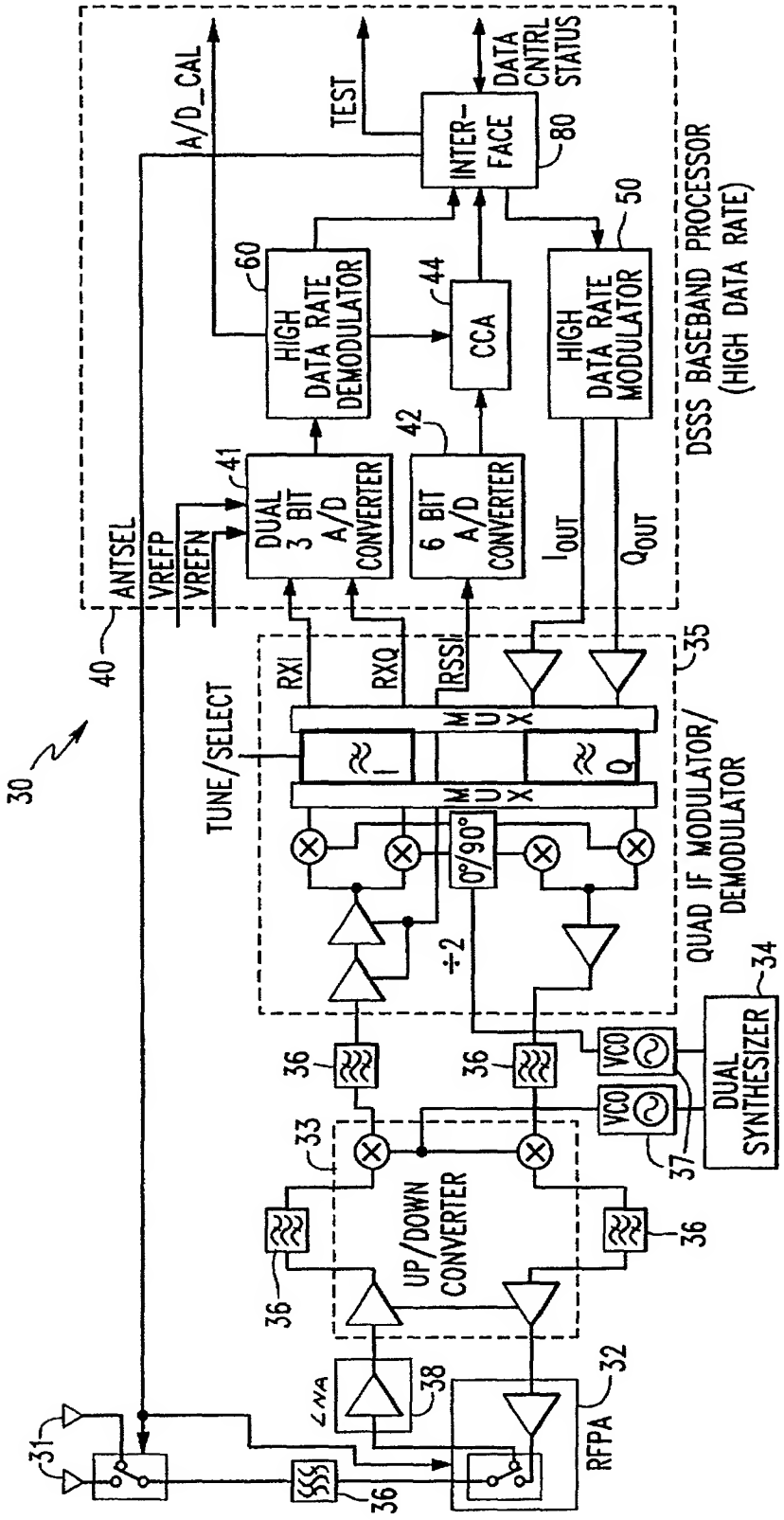
DSSS BASEBAND PROCESSOR (HIGH DATA RATE)
A/D_CAL
TEST
DATA CNTRL STATUS
INTER-FACE
80
50
60
HIGH DATA RATE DEMODULATOR
44
CCA
HIGH DATA RATE MODULATOR
42
41
DUAL 3 BIT A/D CONVERTER
6 BIT A/D CONVERTER
ANTSEL
VREFP
VREFN
I_{OUT}
Q_{OUT}
40
30
RXI
RXQ
RSSI
35
MUX
TUNE/SELECT
I
Q
0°/90°
÷2
QUAD IF MODULATOR/ DEMODULATOR
34
DUAL SYNTHESIZER
VCO
VCO
37
36
33
UP/DOWN CONVERTER
LNA
38
RFPA
32
31

FIG. 1

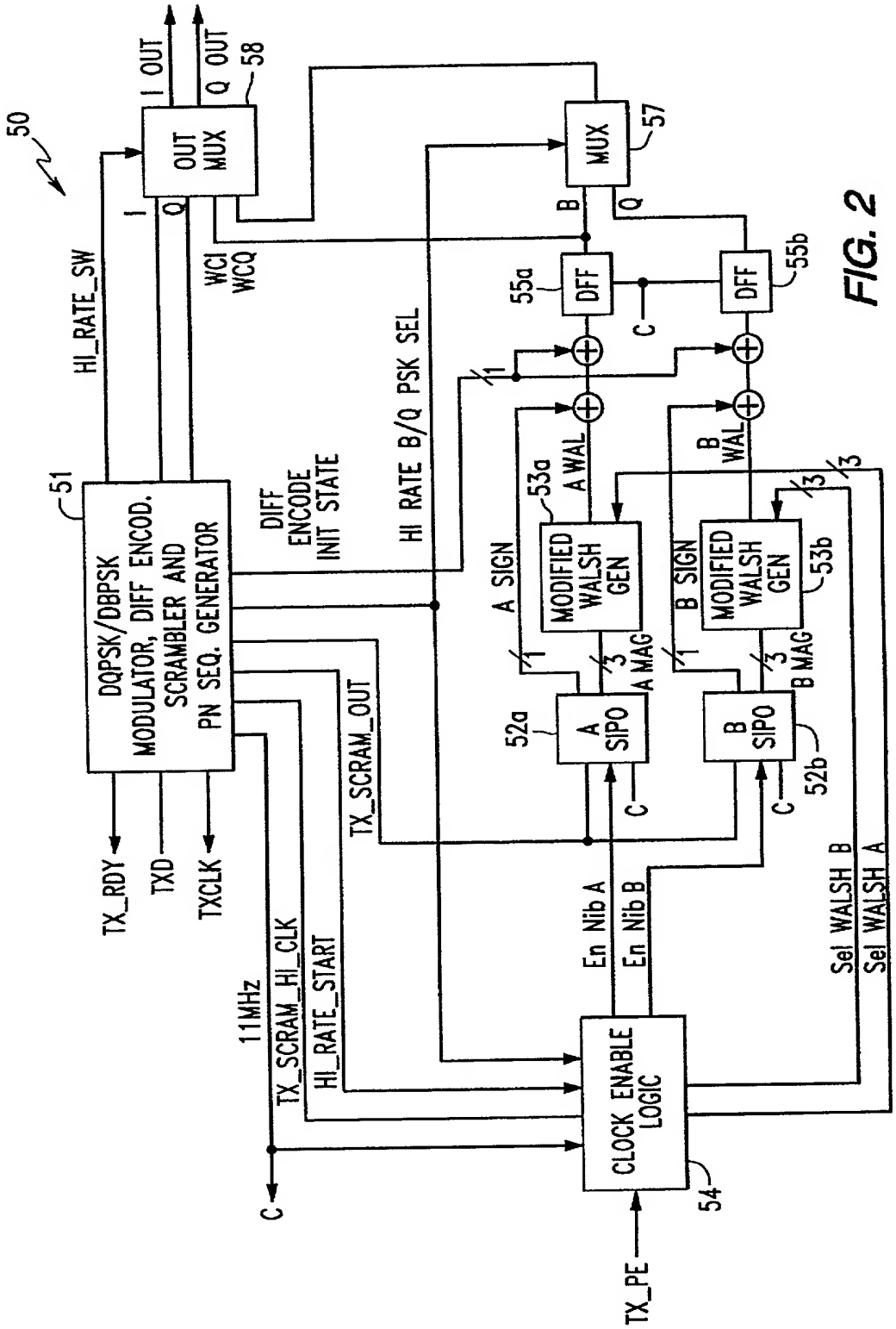
50
I OUT
Q OUT
58
OUT MUX
I
Q
WCI
WCQ
MUX
57
B
Q
HI_RATE_SW
55a
DFF
55b
DFF
C
51
DQPSK/DBPSK MODULATOR, DIFF ENCOD. SCRAMBLER AND PN SEQ. GENERATOR
DIFF ENCODE INIT STATE
HI RATE B/Q PSK SEL
11
A WAL
B WAL
53a
MODIFIED WALSH GEN
53b
MODIFIED WALSH GEN
A SIGN
B SIGN
1
3
A MAG
B MAG
52a
A SIPO
52b
B SIPO
C
TX_RDY
TXD
TXCLK
TX_SCRAM_OUT
11MHz
TX_SCRAM_HI_CLK
HI_RATE_START
C
En Nib A
En Nib B
Sel WALSH B
Sel WALSH A
CLOCK ENABLE LOGIC
54
TX_PE

FIG. 2

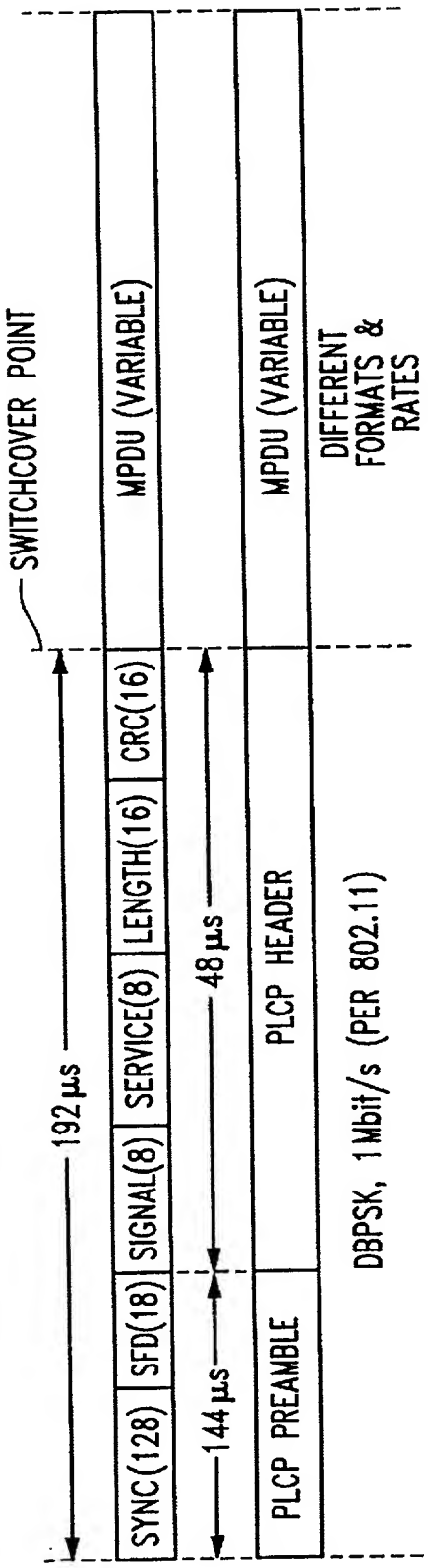
SWITCHCOVER POINT
MPDU (VARIABLE)
MPDU (VARIABLE)
DIFFERENT FORMATS & RATES
SYNC(128)
SFD(18)
SIGNAL(8)
SERVICE(8)
LENGTH(16)
CRC(16)
192 µs
144 µs
48 µs
PLCP PREAMBLE
PLCP HEADER
DBPSK, 1Mbit/s (PER 802.11)

FIG. 3

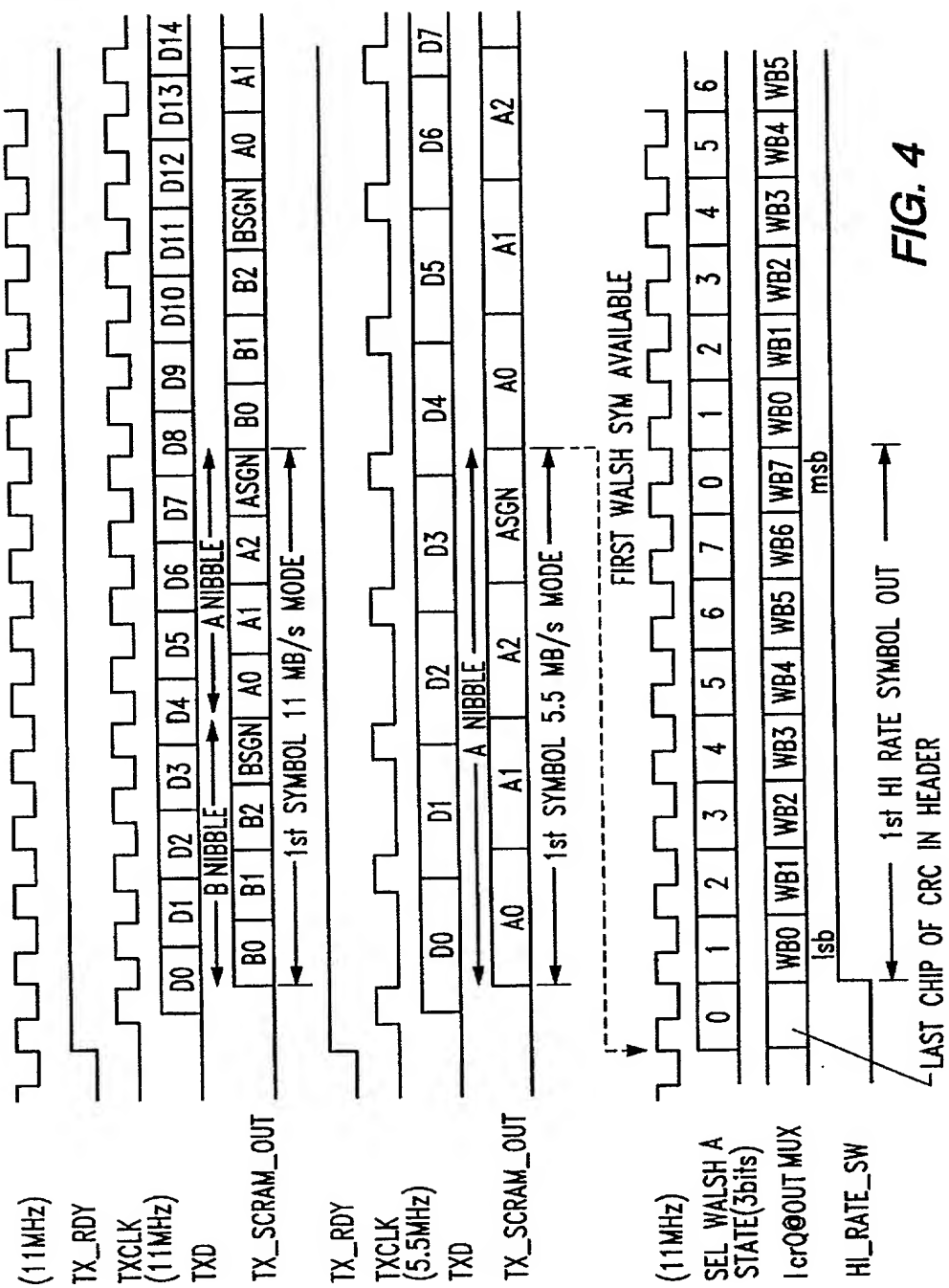
(11MHz)
TX_RDY
TXCLK (11MHz)
TXD
TX_SCRAM_OUT
TX_RDY
TXCLK (5.5MHz)
TXD
TX_SCRAM_OUT
(11MHz)
SEL WALSH A STATE(3bits)
IcrQ@OUT MUX
HI_RATE_SW
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14
B NIBBLE
A NIBBLE
B0 B1 B2 BSGN A0 A1 A2 ASGN B0 B1 B2 BSGN A0 A1
1st SYMBOL 11 MB/s MODE
D0 D1 D2 D3 D4 D5 D6 D7
A NIBBLE
A0 A1 A2 ASGN A0 A1 A2
1st SYMBOL 5.5 MB/s MODE
FIRST WALSH SYM AVAILABLE
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6
WB0 WB1 WB2 WB3 WB4 WB5 WB6 WB7 WB0 WB1 WB2 WB3 WB4 WB5
lsb
msb
1st HI RATE SYMBOL OUT
LAST CHIP OF CRC IN HEADER

FIG. 4

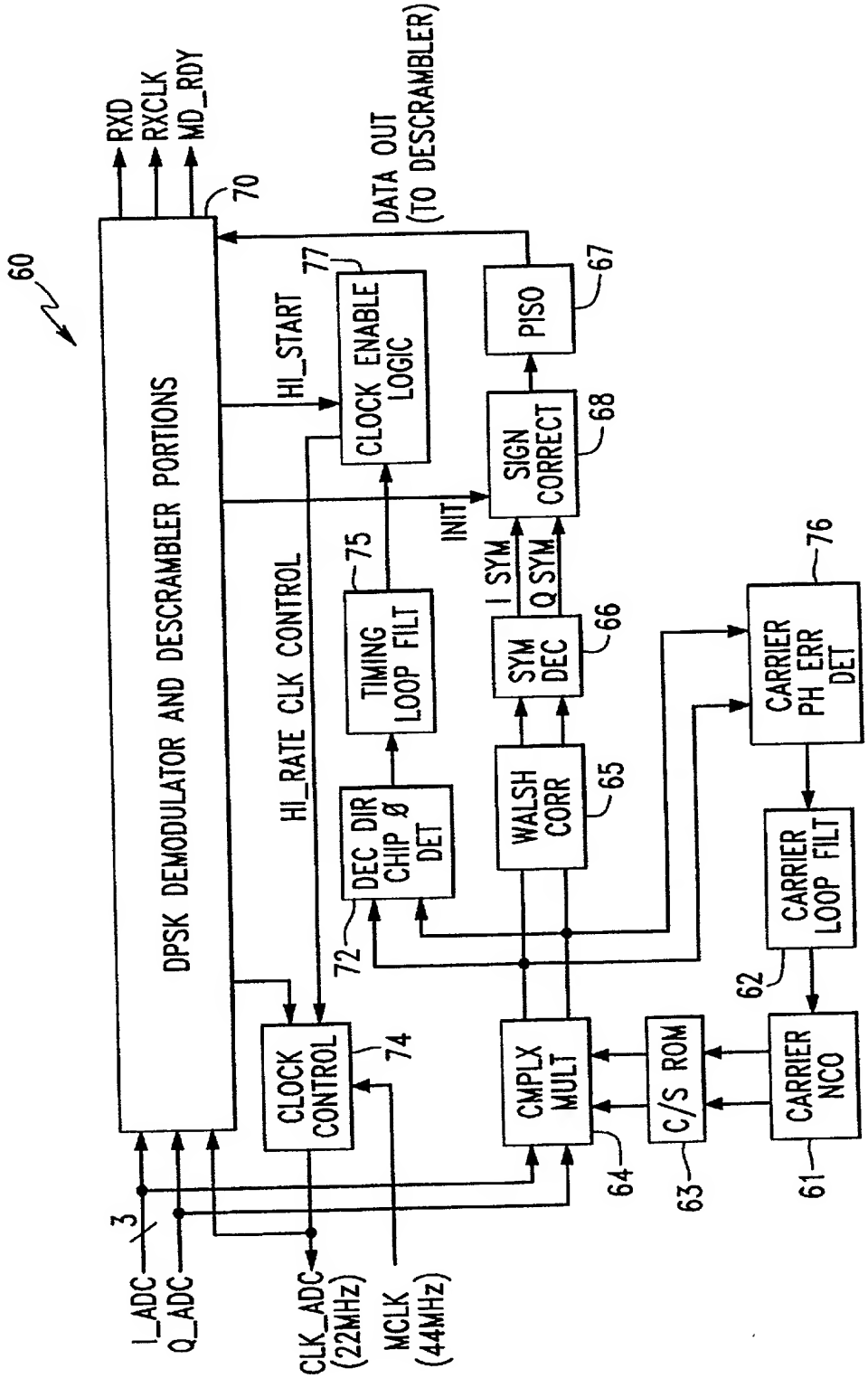
60
DPSK DEMODULATOR AND DESCRAMBLER PORTIONS
70
RXD
RXCLK
MD_RDY
DATA OUT (TO DESCRAMBLER)
67
PISO
68
SIGN CORRECT
77
CLOCK ENABLE LOGIC
HI_START
INIT
I SYM
Q SYM
66
SYM DEC
75
TIMING LOOP FILT
HI_RATE CLK CONTROL
65
WALSH CORR
72
DEC DIR CHIP Ø DET
76
CARRIER PH ERR DET
CARRIER LOOP FILT
62
74
CLOCK CONTROL
CMPLX MULT
64
C/S ROM
63
CARRIER NCO
61
3
I_ADC
Q_ADC
CLK_ADC (22MHz)
MCLK (44MHz)

FIG. 5

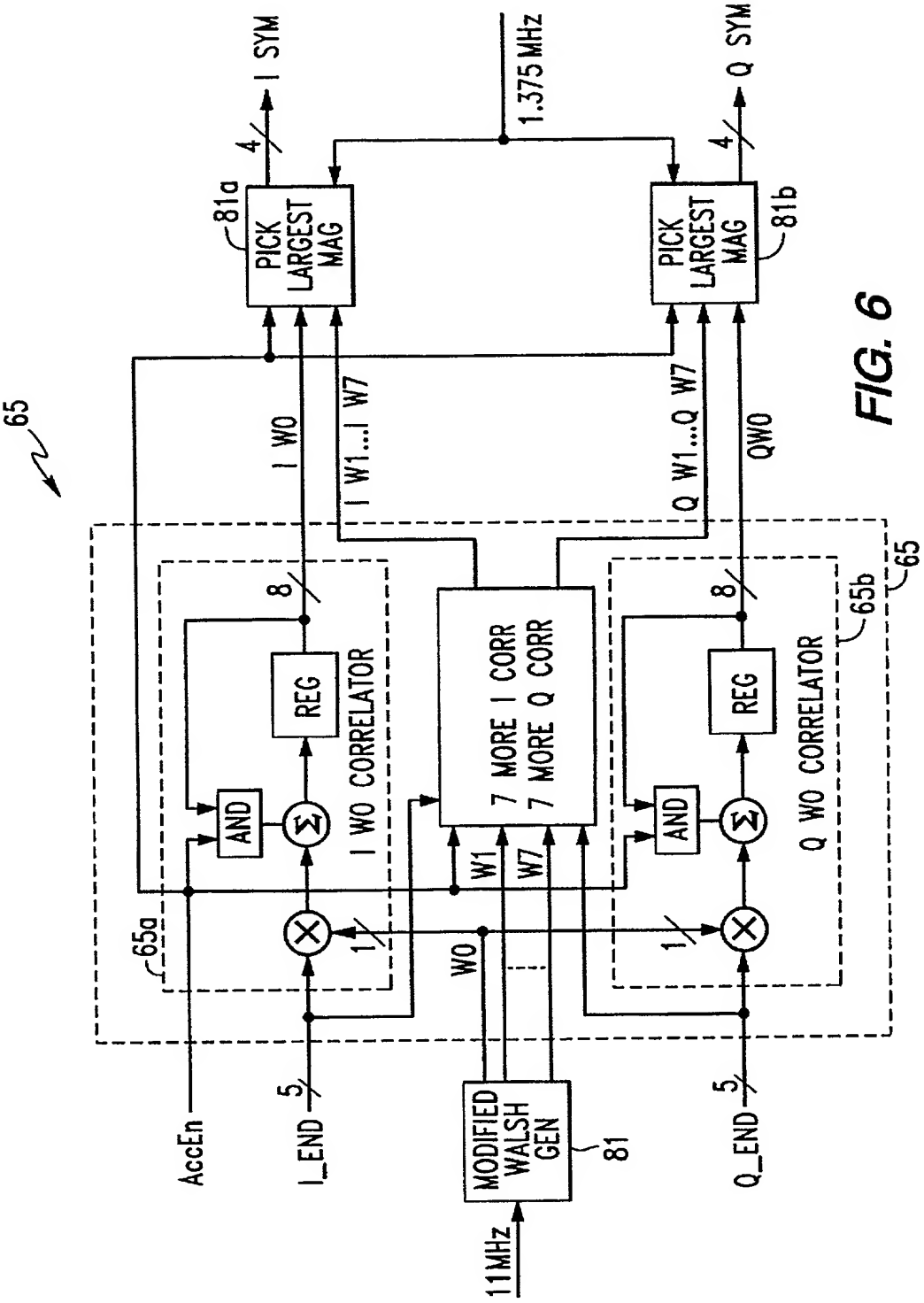
65
I SYM
4
1.375 MHz
Q SYM
4
81a
PICK LARGEST MAG
PICK LARGEST MAG
81b
I W0
I W1...I W7
Q W1...Q W7
QW0
8
8
REG
REG
AND
AND
Σ
Σ
I W0 CORRELATOR
7 MORE I CORR
7 MORE Q CORR
Q W0 CORRELATOR
65a
65b
65
W1
W7
W0
1
1
5
5
AccEn
I_END
Q_END
MODIFIED WALSH GEN
81
11MHz

FIG. 6

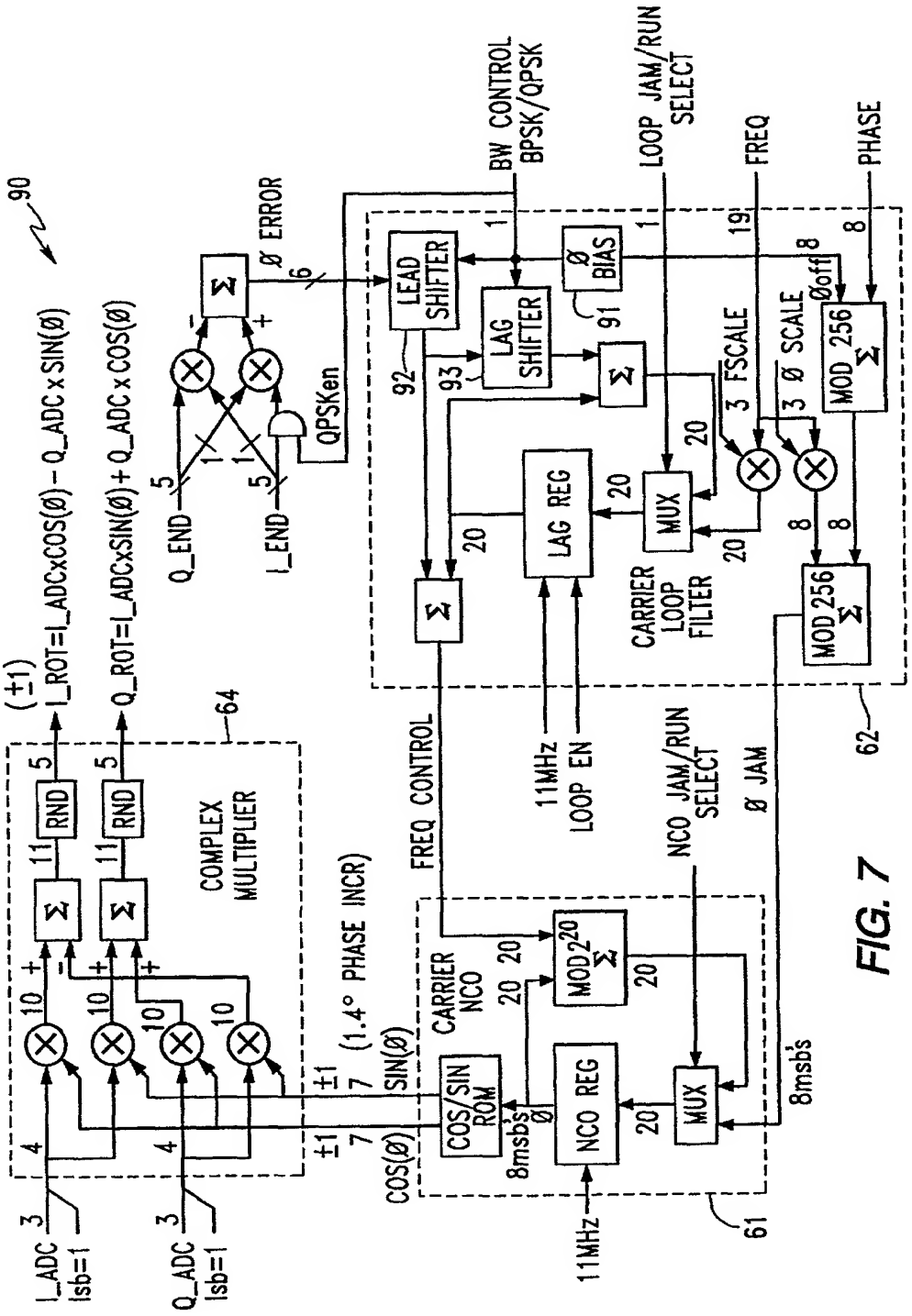
90
I_ADC
Q_ADC
COMPLEX MULTIPLIER
64
I_ROT=I_ADCxCOS(ø) – Q_ADC x SIN(ø)
Q_ROT=I_ADCxSIN(ø) + Q_ADC x COS(ø)
(±1)
RND
Σ
SIN(ø)
COS(ø)
(1.4° PHASE INCR)
FREQ CONTROL
CARRIER NCO
COS/SIN ROM
NCO REG
MOD 2^20
8msb's
11MHz
LOOP EN
NCO JAM/RUN SELECT
ø JAM
61
62
Ø ERROR
Q_END
I_END
QPSKen
BW CONTROL BPSK/QPSK
LOOP JAM/RUN SELECT
FREQ
PHASE
LEAD SHIFTER
LAG SHIFTER
Ø BIAS
LAG REG
MUX
CARRIER LOOP FILTER
FSCALE
Ø SCALE
Øoff
MOD 256

FIG. 7

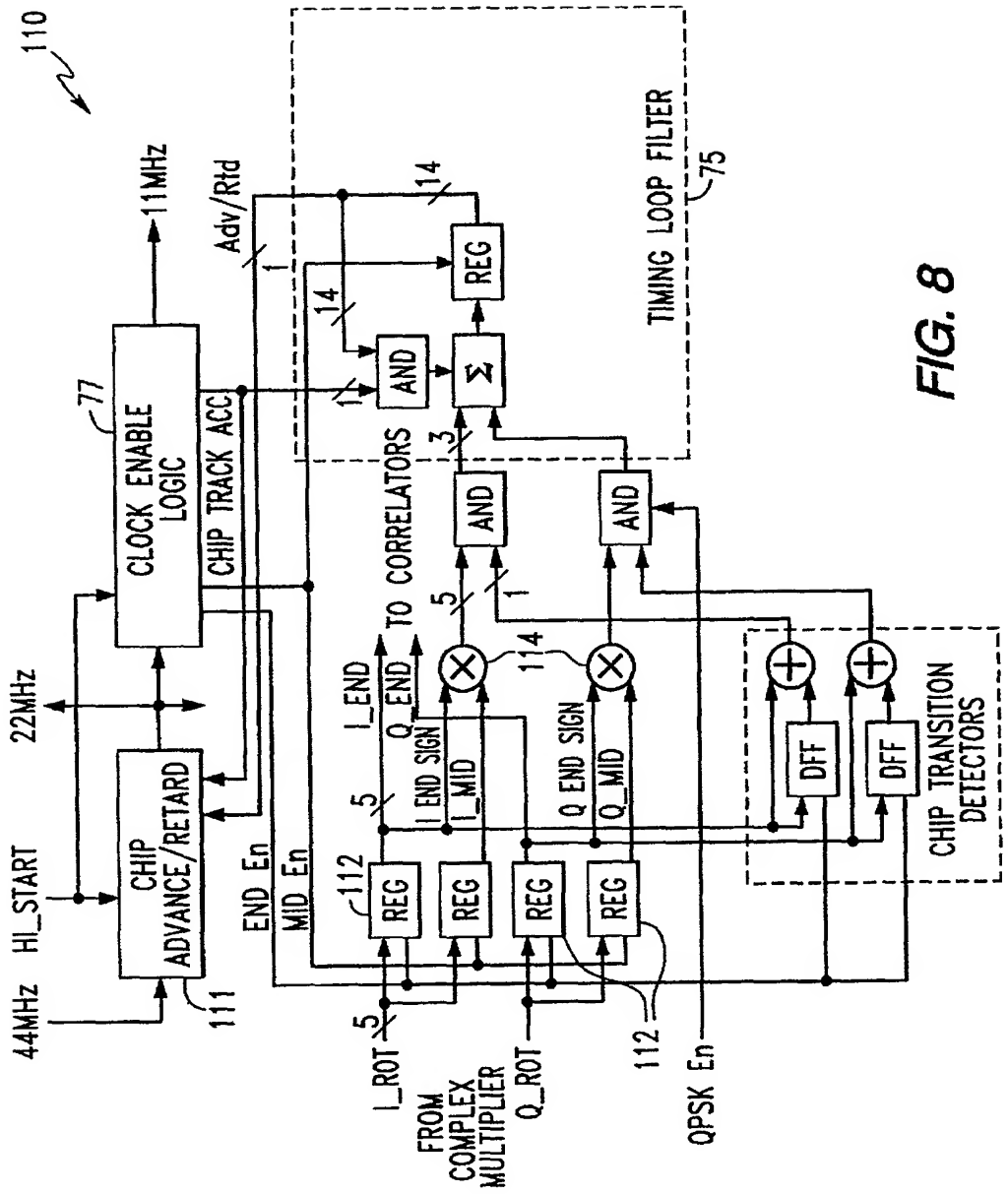
110
11MHz
Adv/Rtd
TIMING LOOP FILTER
75
77
CLOCK ENABLE LOGIC
CHIP TRACK ACC
22MHz
HI_START
44MHz
CHIP ADVANCE/RETARD
111
END En
MID En
112
REG
I_END
Q_END
I END SIGN
I_MID
Q END SIGN
Q_MID
TO CORRELATORS
AND
Σ
114
DFF
CHIP TRANSITION DETECTORS
I_ROT
Q_ROT
FROM COMPLEX MULTIPLIER
QPSK En

FIG. 8